ON APPEAL TO THE U.S. PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:	Ionel D. Jitaru	:	
Serial No.:	10/511,232	:	Examiner: Vu, Bao Q.
Filing Date:	August 4, 2005	:	Art Unit: 2838

Title: **HIGH EFFICIENCY FLYBACK CONVERTER**

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Commissioner for Patents
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Alexandria, VA 22313-1450

APPELLANT'S APPEAL BRIEF

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APPELLANT'S APPEAL BRIEF

This is Appellant's Brief on Appeal pursuant to 35 U.S.C. § 134(a). The following sections of this Brief are the items set forth in 37 C.F.R. § 41.37(c).

Real Party in Interest (37 C.F.R. § 41.37(c) (1) (i))

DET International Holding Limited, a Cayman Islands corporation and assignee of the inventor Ionel D. Jitaru, is the real party in interest.

Related Appeals and Interferences (37 C.F.R. 41.37(c) (1) (ii))

There are no related appeals or interferences.

Status of Claims (37 C.F.R. § 41.37(c) (1) (iii))

Claims 6, 7, 13 – 16, 23, 24 and 33 are rejected.

Claims 1 – 5, 8 – 12, 17 – 22, 25 – 32 and 34 – 38 are withdrawn.

The rejected claims are all of the claims presently being examined in this application. Each is under final rejection. The claims on appeal are appended at Appendix A.

The withdrawn claims are claims that were not selected in a response to a restriction requirement. Of these, claims 8 – 12, 17 – 22, 25 – 32, 34 and 35 are dependent claims

incorporating the limitations of one of the claims on appeal. The withdrawn claims are appended at Appendix C.

Status of Amendments (37 C.F.R. § 41.37(c) (1) (iv))

There are no amendments outstanding.

Summary of Claimed Subject Matter (37 C.F.R. § 41.37(c) (1) (v))

Without limiting the interpretation of the claims on appeal, which claims stand on their own, the invention of the claims in the application relates to the control of a synchronous rectifier (S2 in Fig. 2 of Appellant's drawings) that is used in the secondary circuit of a DC-DC flyback converter (claims 6, 7, 13 – 16) (Fig. 2 and page 7, line 17 – page 8, line 2 of Appellant's specification) and to the DC-DC flyback converter (Fig. 2) with the controlled synchronous rectifier (S2)in its secondary circuit (claims 23, 24 and 33) (page 7, lines 4 – 5). DC-DC flyback converters are well known and widely used power conversion components. As its name suggests, the DC-DC flyback converter converts a first DC input voltage to a second DC output voltage. Components common to all DC-DC flyback converters are a transformer, a switch connected with the primary of the transformer and one or more rectifying diodes connected with the secondary winding of the transformer (page 1, lines 12 – 14). The control method and configurations claimed are for the purpose of reducing losses and hence improving efficiency in power conversion devices of this kind (page 3, lines 1 – 4).

In the flyback converter of the claims on appeal, a synchronous rectifier is the diode used on the secondary side of the transformer, i.e. "the secondary circuit" (page 3, lines 8 – 14).

Independent Claim 6

Independent claim 6 is directed to controlling the synchronous rectifier (S2 in Fig. 2) in a DC-DC flyback converter secondary circuit to reduce losses by (a) turning ON the synchronous rectifier as a result of a voltage being established across the transformer's secondary winding and (b) turning OFF the synchronous rectifier as a result of the primary circuit switch being turned ON (Fig. 3 and page 8, lines 3 – 18).

Independent Claim 23

Independent claim 23 describes the control circuitry (100 in Fig. 3) of the appellant's DC-DC flyback controller (page 8, line 3). More particularly it calls for a DC-DC flyback converter (Fig. 2) in which a control circuit (Fig. 3) is coupled between a primary control signal input connection that applies a first control signal (Vc (S1) of Figs. 2 and 3) to the converter's primary switch (S1) in its primary circuit and a control connection for applying a second control signal (Vc (S2) of Figs. 2 and 3) to converter's synchronous rectifier in its secondary circuit (page 8, lines 5 – 14). The control circuit is further described as a control primary winding (66 in Fig. 5) and a control secondary winding (68 in Fig. 5) wound on the converter's main transformer (page 9, lines 5 – 8). The control primary winding is connected in a circuit (60, 62, 64 in Fig. 5) that has an input from the primary control circuit input connection (60 in Fig. 5, page 9, lines 12 – 14). The control circuit secondary winding (68 in Fig. 5) is connected in controlling relation to the synchronous rectifier (86) control connection (page 9, lines 25 – 32). The claim further sets forth that the main transformer has a magnetic core with a main primary winding wound on a center flux path (72 in Fig. 5, page 10, lines 1 – 4) The control primary winding wound (66) on at least one of two outer flux paths (70 and 74, page 9, lines 16 – 20). And the control secondary winding is wound on the two outer flux paths (70 and 74) so as to be in current cancelling relation with respect to flux conducted to the two outer flux paths from the center flux path (page 9, lines 15 – 19). This main transformer configuration and secondary control winding makes the secondary control winding substantially unaffected by flux developed by currents in the main primary winding (page 9, lines 24 and 25).

Independent Claim 33

Using means plus function terms of the kind sanctioned by 35 U.S.C. § 112, sixth paragraph, independent claim 33 claims a DC-DC flyback converter (Fig. 2) controlled in the manner set forth in independent claim 6 as described above. The claim calls for a control circuit (Figs. 2 and 3) coupled between (a) the converter's control switch (S1) connected with the primary winding and (b) the synchronous rectifier (S2) of the secondary circuit (page 8, line 3). The control circuit includes (a) means for turning ON the synchronous rectifier in dependence on a voltage developed across a secondary winding on the main transformer (comparators 102 and

106 and bi-stable circuits 112 and 114 with inverter 101 of Fig. 3, page 8, lines 3 – 18), and (b) means for turning OFF the synchronous rectifier in dependence on a first control signal turning ON the controllable switch of the primary circuit (inverter 101, page 8, lines 14 – 18).

Claims Dependent from Claim 6

Claim 7 is dependent from claim 6 and is directed to a preferred embodiment in which the synchronous rectifier is turned OFF in dependence on a control signal (Vc (S1), Fig. 3) turning ON the primary or "main" switch (S1, Fig. 3, page 8, lines 3 – 5 and 16 – 17).

Claim 13 is dependent from claim 6 and recites the steps of winding a main transformer with three flux paths as described above with respect to independent apparatus claim 23 (Fig. 5, paths 70, 72, 74, page 9, lines 15 – 20).

Claim 14, dependent form claim 13, calls for winding the main secondary winding on the center flux path (Fig. 5, path 72, page 9, lines 15 – 16).

Claim 15, dependent from claim 13, calls for winding a control primary winding on the two outer flux paths in flux cancelling relation with respect to the center flux path (Fig. 5, winding 68, paths 70, 72, 74, page 9, lines 20 – 21).

Dependent from claim 13, claim 16 calls for the application of a control voltage from the control secondary winding (Fig. 5, 68) to switch ON and OFF the synchronous rectifier (82, page 9, lines 25 – 32).

Claim 24, Dependent from Independent Claim 23

Dependent claim 24 adds to the recitations of claim 23 that the control primary winding (Fig. 5, winding 66) is wound on the two outer flux paths (70 and 74) in flux cancelling relation with respect to the center flux path (page 9, line 20).

Grounds of Rejection to be Reviewed on Appeal (37 C.F.R. § 41.37(c) (1) (vi))

Claims 6, 7, 13 – 16 and 33 stand finally rejected under 35 U.S.C. § 102(e) as anticipated over U.S. patent No. 6,418,039 of Lentini et al.

Claims 13 – 15, 23 and 24 stand finally rejected under 35 U.S.C. § 103(a) as unpatentable over the Lentini et al. patent in view of U.S. patent No. 6,400,579 of Cuk.

Argument (37 C.F.R. § 41.37(c) (1) (vii))

The present application relates to control of a DC-DC flyback converter. An important feature of the control is to eliminate or nearly eliminate (1) power losses due to cross-conduction between a main, controllable switch in a primary circuit of the converter and a secondary circuit's synchronous rectifier and (2) reverse recover losses, both of which losses DC-DC flyback converters are subject to. See specification page 6, lines 9 – 12. This is accomplished by a control circuit that processes in a sequence information relating to control of the primary's main switch, voltage across a secondary winding of a power transformer, and voltage across the synchronous rectifier. From this a final control signal is obtained for the synchronous rectifier that accomplishes the above loss reductions or eliminations. Specification page 3, lines 8 – 13. In the embodiment at issue the synchronous rectifier is turned ON in dependence on the establishment of a voltage across the secondary winding of the converter's main transformer and the synchronous rectifier is turned OFF in dependence on the turning ON of the main switch in the primary circuit. Specification page 4, lines 8 – 15. Claims 6, 7, 13 – 16 and 33 relate to controlling the converter in the above manner.

The Lentini et al. patent does not describe "each and every element" of the independent claims 6 and 33 and so cannot be said to anticipate these claims or the claims 7 and 13 – 16 that include the elements of claim 6 by their dependency. See *Verdegard Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631 (Fed. Cir. 1987) (cited with approval in Manual of Patent Examination Procedure, § 2131 (p. 21009-67)).

As regards the rejection over Lentini et al. combined with Cuk, because the Cuk patent relied upon in combination with the Lentini et al. patent does not teach those elements of independent claim 6 lacking in the Lentini et al. patent, the teachings of the two patents cannot be combined to arrive at the content of claims 13 – 15, dependent from claim 6. In addition, the two patents each fail to teach or suggest the transformer winding arrangements of these dependent claims. As for claims 23 and 24, neither patent teaches the transformer winding

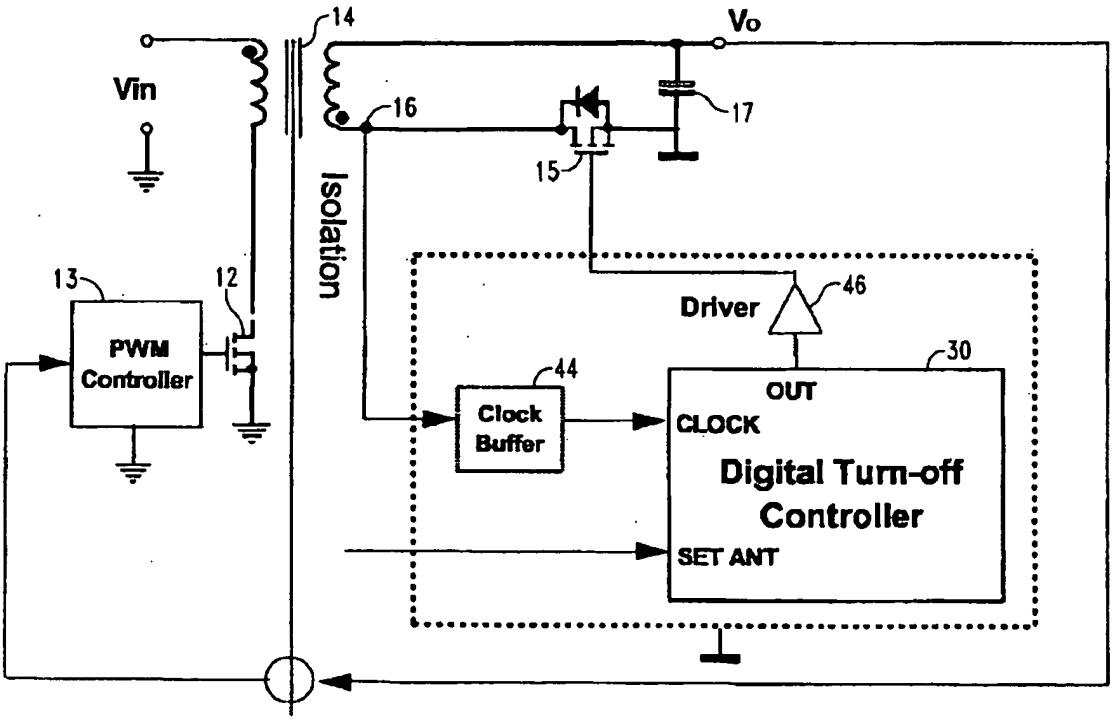
arrangement of these claims. Claims 13 - 15, 23 and 24, then, were not obvious over the Lentini et al. and Cuk patents at the time of the invention. Consequently, the burden of presenting a prima facie case of unpatentability under 35 U.S.C. § 102 or 35 U.S.C. § 103 has not been met by the examiner in this application and all of the rejected claims should now be allowed and the appellant awarded the patent to which he is entitled. In re *Glaug et al.*, 283 F.3d 1335, 1338 (Fed. Cir., 2002).

Independent Claims 6 and 33 are Patentable Over Lentini et al.

In the final rejection based on the Lentini et al. patent, the examiner states:

> Claim 6, 7, 13 – 16 and 33 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Lentini et al. (USP 6,418,039). Lentini discloses a flyback converter (14) with a digitally controlled synchronous rectifier (15).

The examiner then reproduces Fig. 21 of Lentini et al.:



Neither the final Official Action nor any prior Official Action actually attempts to apply the disclosure of the Lentini et al. patent to any claim said to be anticipated.

The Lentini et al. Fig. 21 does, in fact, depict a DC-DC flyback converter. Lentini et al. column 10, lines 44 – 50. Lentini et al. explain that the method of control of synchronous rectifiers described is "being implemented by "STMicroelectronics, S.r.l., in the design of a silicon device family ...." Lentini et al., column 10, lines 31 – 33. Most of the descriptions and drawings of Lentini et al. relate to converters with two synchronous rectifiers in the secondary circuit controlled by two output OUT_1 and OUT_2 of control circuit. However, referring to the STMicroelectronics IC, STSR3, Lentini et al. state that the Fig. 21 implementation (shown above) uses the previously described control system, "but only for the part relative to OUT_2." Lentini et. Al., column 10, lines 45 – 47. Appellant points this out because to determine if the Fig. 21 flyback controller of Lentini et al. effects the method of method claims 6, 7 and 13 – 16 or is configured as set forth in apparatus claim 33 it is necessary to understand whether Lentini et al. control the output OUT_2 of the digital controller 30 of Fig. 12 of Lentini et al. such that this application's claims 6, 7, 13 – 16 and 33 are anticipated.

Independent claim 6 requires, inter alia:

> turning OFF the synchronous rectifier in dependence on turning ON of a main switch in the primary circuit in current controlling relation to a primary winding of the main transformer.

Lentini et al. do not do that. Independent claim 33 requires:

> means for turning OFF the synchronous rectifier in dependence on the first control signal turning ON the controllable switch.

The Lentini et al. DC-DC converter does not have that.

Appellant's Figs. 2 and 3 show the digital control circuit 100 connected between the switching control input Vc (S1) of the primary switch S1 and the switching control Vc (S2) of the switch S2 that is the synchronous rectifier.

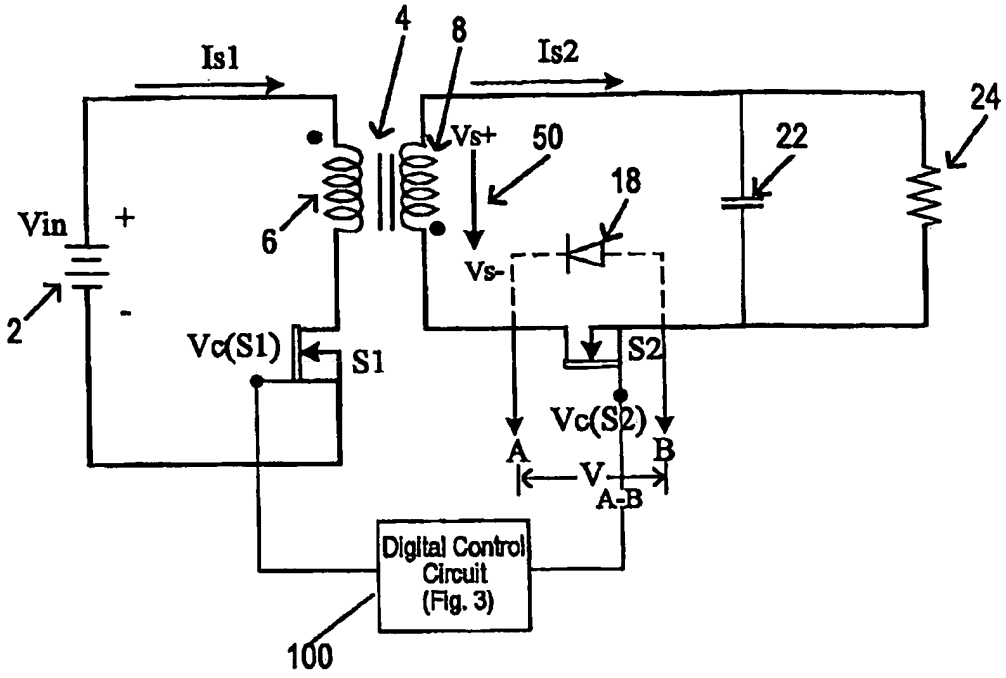

Is1
Is2
4
8
24
22
Vs+
50
18
Vin
+
-
6
2
Vs-
Vc(S1)
S1
S2
Vc(S2)
A
B
V
A-B
Digital Control Circuit (Fig. 3)
100

Fig. 2

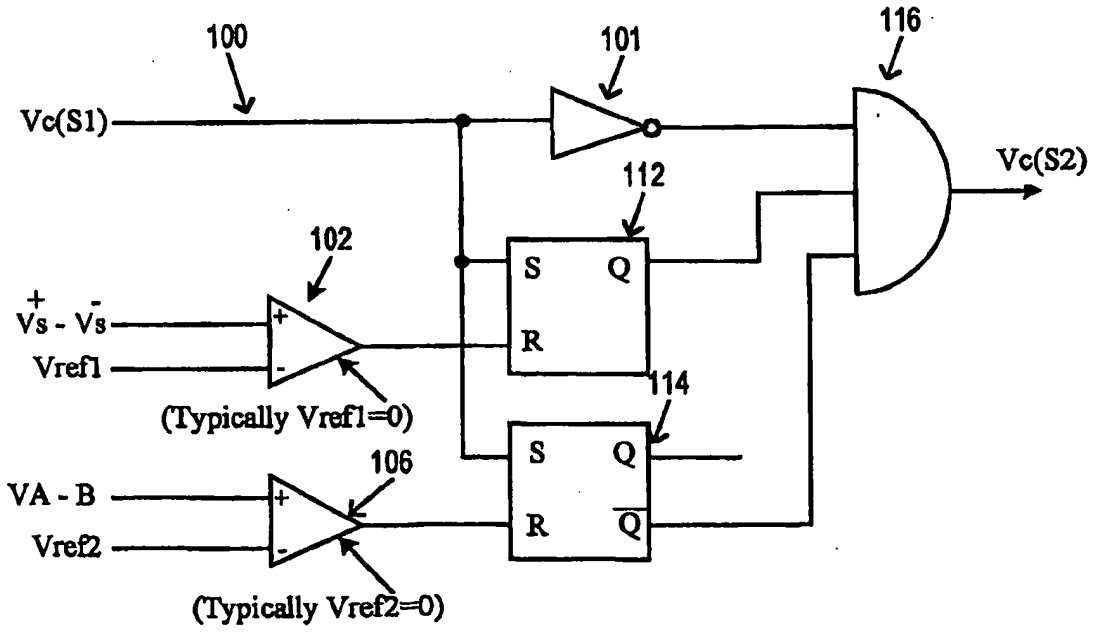

100
101
116
Vc(S1)
Vc(S2)
112
102
S
Q
R
Vs - Vs
Vref1
(Typically Vref1=0)
114
106
VA - B
Vref2
(Typically Vref2=0)

Fig. 3

These show the implementation of the above-quoted step (b) of claim 6 and they are also significant in interpreting the above-quoted means plus function language of claim 33 in accordance with 35 U.S.C. § 112, sixth paragraph.

Compare the figure from the Lentini et al. patent that the examiner reproduces in the final Official Action, Fig. 21 reproduced above. There, no signal is communicated from control 13 for the primary switch 12. Rather, it is a signal taken from the secondary of the isolation transformer 14 at node 16 that is buffered at 44 to become the clock signal that, along with a SET ANT (set anticipation period) signal, is used in calculating the turning ON and OFF of the Lentini et al. synchronous rectifier 15. Lentini et al., column 7, line 66 – column 8, line 7.

While the clock signal input taken from the secondary at node 16 is "related to the main PWM [pulse width modulation] signal of switch-node circuit [primary switch], that clock signal does not turn on and off the secondary circuit synchronous rectifier, but rather is used to calculated the turning OFF of that synchronous rectifier a cycle later. Lentini et al. column 8, lines 18 – 27 and column 9, lines 3 – 13. Moreover, because an anticipation time is also used in calculating the turning ON and OFF of the next cycle the secondary circuit synchronous rectifier is not turned OFF "in dependence on the first control switch turning ON the controllable switch" in the primary, but, rather, the synchronous rectifier in the secondary circuit is turned OFF before the primary circuit's switch is turned ON. Lentini et al., column 9, lines 3 – 18. This is illustrated graphically in the timing diagram Fig. 13 of Lentini et al.

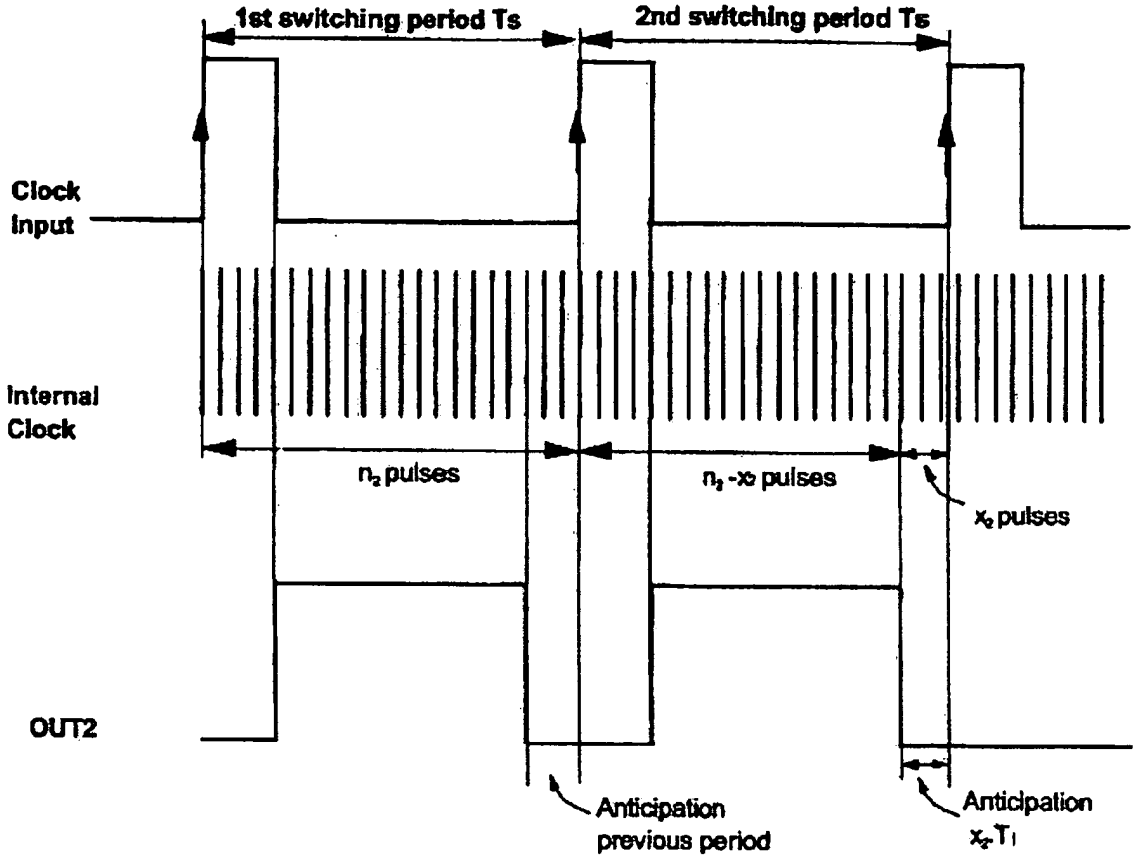


Fig. 13

OUT2 is shown dropping at a time that is an anticipation period prior to the clock input rise. So even if the clock input represented the turning ON and OFF of the main switch in the primary circuit (which it does not), the synchronous rectifier controlled by OUT_2 is not turned OFF in dependence on switching on the main switch, but rather in anticipation based on the measured last cycle of the converter. Independent claims 6 and 33 are not anticipated by the Lentini et al. patent and their rejection should be overturned.

Dependent Method Claims 7 and 13 – 16 Are Not Met by Lentini et al.

Dependent claim 7 calls for "turning OFF the synchronous rectifier in dependence on a control signal turning ON the main switch." Operating as explained above, the Lentini et al.

patent does not meet this further provision and claim 7 is patentable over Lentini et al. for this reason as well as its dependency from claim 6.

Dependent claim 13 calls for:

> the secondary winding is a control secondary winding, steps (a) comprising providing in the main transformer a magnetic core having a center flux path and two outer flux paths, winding the control secondary winding on the two outer flux paths in current canceling relation as to flux conducted to the two outer flux paths from the center flux path, winding a control primary winding on at least one of the two outer flux paths, winding on the center flux path at least a main primary winding in energy communicating relation to a main secondary winding.

Nothing of this nature appears anywhere in Lentini et al. In rejecting claim 13 as anticipated by Lentini et al., the final Official Action never treats the provisions of claim 13. This claim is patentable over Lentini et al. for the above-quoted content as well as for its dependence from claim 6.

Claim 14, dependent from claim 13, calls for "winding the main secondary winding on the center flux path." Claim 15, dependent from claim 13, calls for "wherein winding a control primary winding comprises winding the control primary winding on the two outer flux paths in flux canceling relation with respect to the center flux path." And claim 16, dependent from claim 13, calls for "applying a control voltage developed in the control secondary winding to control the switching ON and OFF of the synchronous rectifier." None of the provisions of claims 14, 15 and 16 can be found in Lentini et al. and these claims are patentable over Lentini et al. for these provisions as well as for their dependency.

Claims 13 – 15, 23 and 24 Patentably Differ from the Combination of Lentini et al. and Cuk

Dependent method claims 13 – 15 are rejected as unpatentable under 35 U.S.C. § 103(a) over the Lentini et al. patent and the U.S. patent No. 6,400,579 of Cuk as well as being rejected an anticipated by the Lentini et al. patent. Independent apparatus claim 23 and dependent apparatus claim 24 are rejected over the Lentini et al. and Cuk patents also.

As pointed out above, one way in which claims 13 – 16 differ from Lentini et al. is by their dependency from claim 6. Cuk does not teach the turning OFF of the synchronous rectifier in dependence on turning ON of the main switch in the primary circuit of a DC-DC converter.

Most of the converters of Cuk do not employ a "main transformer inductively coupling the secondary circuit to a primary circuit" as claim 6 requires. However, the converters of Figs. 35b, 36a, 36b and 38a – 38h, 39a – 39c, 40, 41a, 41b, and 42 do employ an isolation transformer coupling primary and secondary circuits. In relation to none of these (nor any other converter shown by Cuk) is there taught turning off a secondary switch or synchronous rectifier in dependence of turning on a main switch in the primary circuit. Since neither of the two relied-upon patents suggest this, there is no basis for contending that any claims dependent from claim 6 (as are claims 13 – 16) are obvious over Lentini et al. and Cuk.

In the final rejection the examiner cites the Cuk patent for flux cancellation in a core:

> Cuk discloses that it is know in the art to provide the use of flux cancellation with the use of flyback converters. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to provide the method and apparatus to digitally control turn-off time of synchronous rectifiers in isolated topologies for switched mode power supplies of Lentini with the use of flux cancellation with the use of flyback converters of Cuk, in order to provide a high efficiency as well as low component stresses for increased converter reliability.

Final Official Action, page 3.

Cuk does teach flux cancellation, for example in the "EE-like core structure ... in Fig. 39c." Cuk, column 37, lines 11 – 13. However, all of Cuk's flux cancellation is taught for avoiding core saturation by DC flux levels in cores coupled to an input and an output inductor L_1 and L_2. However, claim 13, and by their dependency claims 14 and 15, calls for "winding the control secondary winding on the two outer flux paths in current cancelling relation as to flux conducted to the two outer paths from the center flux path."

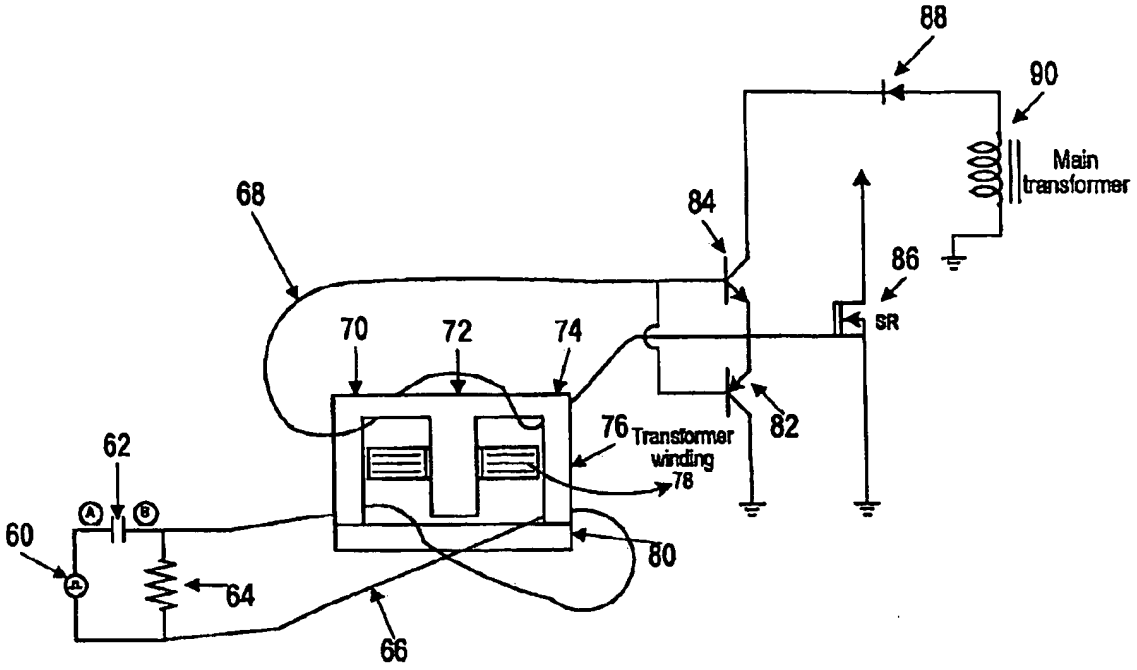


Fig. 5

As shown in appellant's Fig. 5 the control primary winding 66 and the control secondary winding 68 are each wound so that flux emanating from the middle leg of the E – I core is in current, not flux, cancellation relation. The distinction was pointed out in the Response to Official Action dated January 14, 2009, but was ignored in the final Official Action of March 17, 2009. The final Official Action of March 17, 2009 only repeated, verbatim, at paragraph 4, page 3, the rejection of the previous Official Action.

It is noteworthy, too, that claim 13, and by their dependencies, claims 14 and 15, speaks to how the "control secondary winding" is wound on the two outer flux paths. In no instance does Cuk wind a control secondary winding on two outer flux paths, let alone in current cancellation relation as regards flux from the middle flux path. Only Fig. 41b of Cuk shows a "control winding," i.e. a winding used to control a primary switch or secondary synchronous rectifier. There is no suggestion in Cuk that the control windings at N_d in Cuk's Fig. 41b are wound as called for in claim 6. See column 38, lines 1 – 16 of Cuk for the only discussion of the converter of Fig. 41b. Moreover, in those embodiments of Cuk in which an inductor *is* wound on outer flux paths of a three-flux path core, the windings are in current additive, not cancelling relation to a flux from the central flux path. See Cuk's Figs. 34 and 39c. Clearly, claim 13, and

claims 14 and 15, dependent from claim 13, were not obvious from Lentini et al. and Cuk at the time of appellant's invention. This rejection should be overturned.

Claim 15, it is noted, does speak of "flux" cancellation as respects the central flux path. Again the description is as to a control winding unlike Cuk. So Cuk does not suggest the content of this claim.

Rejected as unpatentable over Lentini et al. and Cuk, apparatus claim 23, like claim 13, and by its dependence claim 24, calls for "the control secondary winding being wound on the two outer flux paths in current canceling relation with respect to flux conducted to the two outer flux paths from the center flux path." For the reasons set forth above respecting claim 13's similar recitation, claim 23 and dependent claim 24 cannot be said to have been obvious over Lentini et al. in view of Cuk at the time of the invention. The rejection is in error and should now be overturned.

Claim 23 goes on to say "whereby a control signal generated in the control secondary winding is substantially unaffected by flux developed in the main transformer by currents in the main primary winding." Thus the claim is further distinguished form and unobvious over the combination of the Lentini et al. and Cuk patents and is patentable over the combination by this.

Claim 24, like claim 15, adds that the control primary winding is wound on the two outer flux paths "in flux canceling relation with respect to the center flux path." The comments above, respecting claim 15 in this regard apply and claim 24 is patentable over Lentini et al. and Cuk for this reason as well.

The Withdrawn Dependent Claims

By their dependency withdrawn claims 8 – 12 and 17 – 22 incorporate the content of claim 6 and should now be allowed. By their dependency, claims 25 – 32 incorporate the content of claim 23 and should now be allowed. And by their dependency, claims 34 and 35 incorporate the content of claim 33 and should now be allowed.

The Non-enabling Lentini et al. Disclosure

Aside from failing to teach the elements of the claims of this application, appellant submits that the Lentini et al. patent is unavailable as prior art because its disclosure is non-enabling.

The Lentini et al. patent describes digital control of synchronous rectifiers in "switched mode power supplies," such as DC-DC converters, where a transformer isolates the primary circuit from the secondary circuit. A digital controller 30 for synchronous rectifiers in the secondary circuit is diagrammed schematically in Fig. 12 of Lentini et al., shown below. A control entity which is said to be a "finite states machine" 34 is described as cooperating with a set of up/down counters 36, 37, 38, 39. The digital controller 30 determines when the one or more synchronous rectifiers in the secondary circuit are switched into and out of conduction.

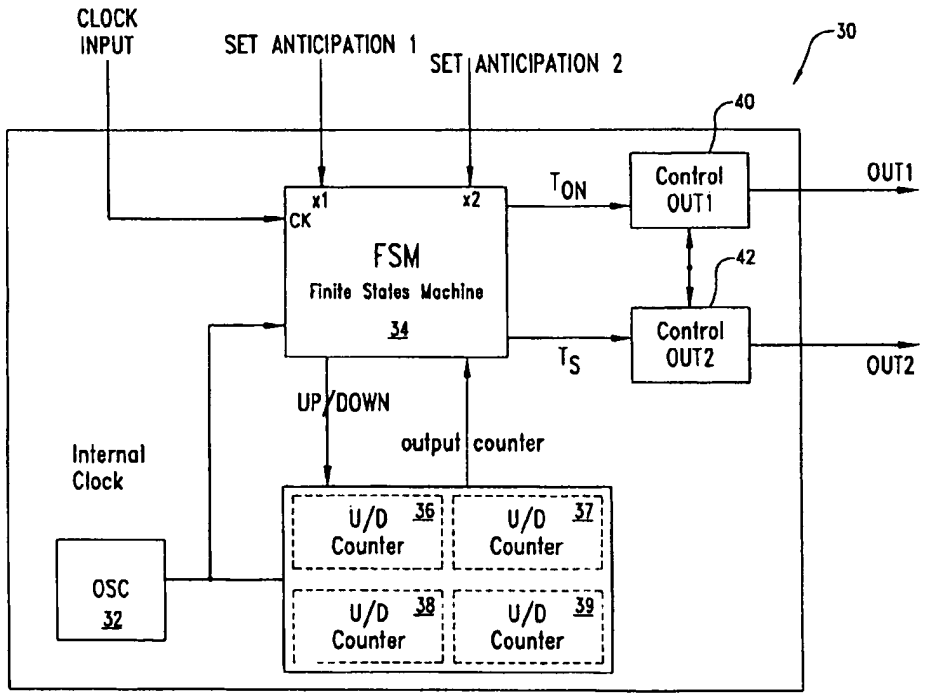


Fig. 12

A "finite states machine" is understood to be not actually a physical component, but rather an analytical construct used, for example, to graphically depict operations or desired operations of a circuit, computer or computer program. See A. Ralston, E. Reilly and D. Hemmendinger, *Encyclopedia of Computer Science*, 4th Ed., 2000, Nature Publishing Grp., London, U.K., 1565-69 (copy attached at Appendix E). For this reason Fig. 12 of the Lentini et al. patent does not make clear the actual circuitry used to accomplish the control described in the patent. In this respect the Lentini et al. patent not only fails to meet the terms of claim 6, but the patent is not a sufficient teaching or enabling reference to teach one of ordinary skill in the art to make and use the digital controller that it refers to.

Also in the Lentini et al. patent, each diagram of a power supply (Figs. 6, 8, 10, 20, 21 and 21) shows a symbol that implies a relationship between the primary circuit, transformer and secondary circuit that is not believed to be an accepted symbol for a circuit element. The apparently non-standard symbol is the arrow connected to the output Vo and pointing to a circle that may be a sensing winding connected with the controller 13 for the primary switch 12. See the encircled portion of Fig. 21 marked "X" below. From the description of the control of Lentini et al., it is clear that the arrow shown is not an element used in the control of either the primary main switch or the secondary circuit synchronous rectifier. In this regard too the Lentini et al. patent appears to be so unclear as not to qualify as an enabling prior art reference. In the appellant's January 14, 2009 Response to an Official Action, the examiner was requested to provide documentary support for (a) how the "finite states machine" of the Lentini et al. controller can be accomplished, and (b) the identity and function of the circuit diagram feature indicated at "X" below. This request went unanswered.

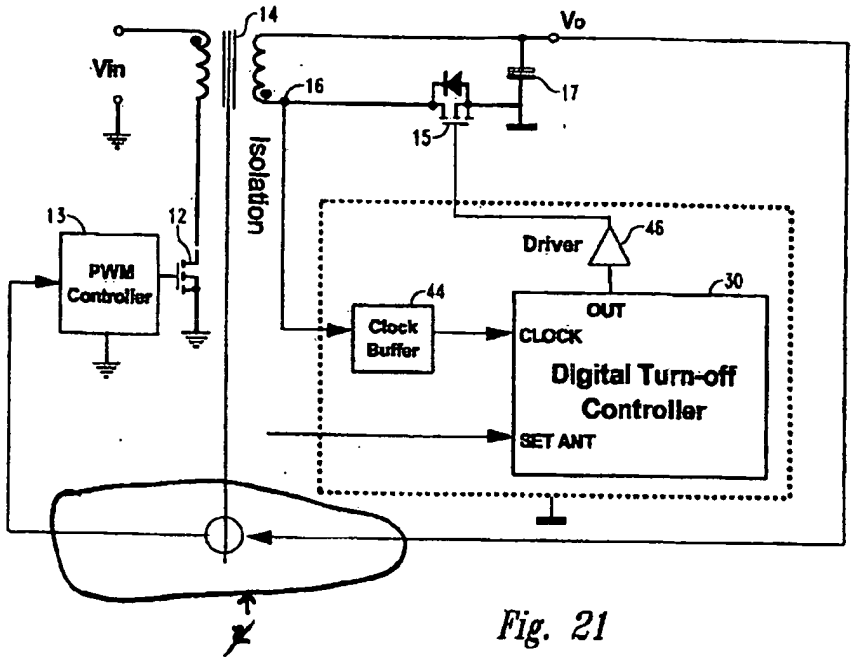


Fig. 21

Conclusion

For reasons expressed above the rejections of claims 6, 7, 13 – 16, 24 and 33 in this application are unfounded and should be reversed. Withdrawn claims 8 – 12, 17 – 22, 25 – 32, 34 and 35 are allowable by their dependency. The Board's review and determination to that end and allowance of the application is respectfully solicited.

Respectfully submitted,

GALLAGHER & KENNEDY

Date: September 11, 2009

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APPENDIX A

Claims on Appeal, 37 C.F.R. § 41.37(c) (1) (viii)

6. A method of controlling conduction of a synchronous rectifier in a secondary circuit of a DC-DC flyback converter comprising:

(a) turning ON the synchronous rectifier in dependence on the establishment of a voltage across a secondary winding of a main transformer inductively coupling the secondary circuit to a primary circuit of the flyback converter, and

(b) turning OFF the synchronous rectifier in dependence on turning ON of a main switch in the primary circuit in current controlling relation to a primary winding of the main transformer.

7. The method according to claim 6, wherein step (b) comprises turning OFF the synchronous rectifier in dependence on a control signal turning ON the main switch.

13. The method according to claim 6, wherein the secondary winding is a control secondary winding, steps (a) comprising providing in the main transformer a magnetic core having a center flux path and two outer flux paths, winding the control secondary winding on the two outer flux paths in current canceling relation as to flux conducted to the two outer flux paths from the center flux path, winding a control primary winding on at least one of the two outer flux paths, winding on the center flux path at least a main primary winding in energy communicating relation to a main secondary winding.

14. The method according to claim 13, further comprising winding the main secondary winding on the center flux path.

15. The method according to claim 13, wherein winding a control primary winding comprises winding the control primary winding on the two outer flux paths in flux canceling relation with respect to the center flux path.

16. The method according to claim 13, further comprising applying a control voltage developed in the control secondary winding to control the switching ON and OFF of the synchronous rectifier.

23. A DC-DC flyback converter having a main transformer, a DC input connection in a primary circuit connected with a primary winding of the main transformer, a controllable primary switch in series with the primary winding of the main transformer, said controllable primary switch having a primary control signal input connection for applying a first control signal in controlling relation to the controllable primary switch, a load connection in a secondary circuit connected with a secondary winding of the main transformer, a synchronous rectifier connected in series with the secondary winding and having a control connection for applying a second control signal to the synchronous rectifier in controlling relation to the synchronous rectifier, a control circuit coupled between the primary control signal input connection and the control connection for applying the second control signal to the synchronous rectifier control connection, the improvement comprising:

the control circuit comprising a control primary winding and a control secondary winding wound on the main transformer, the control primary being connected in a circuit having an input from the primary control signal input connection, the control secondary winding being connected in controlling relation to the control connection of the synchronous rectifier, the main transformer having a magnetic core with a center flux path on which is wound a main primary

winding, and the magnetic core having two outer flux paths on both of which is wound the control secondary winding, the control primary winding being wound on at least one of the outer flux paths, the control secondary winding being wound on the two outer flux paths in current canceling relation with respect to flux conducted to the two outer flux paths from the center flux path, whereby a control signal generated in the control secondary winding is substantially unaffected by flux developed in the main transformer by currents in the main primary winding.

24. The DC-DC flyback converter of claim 23, wherein the control primary winding is wound on both of the two outer flux paths in flux canceling relation with respect to the center flux path.

33. A DC-DC flyback converter having a main transformer, a primary circuit including a controllable switch connected in current controlling relation to a primary winding and having a control connection for opening and closing the switch under the control of a first control signal, a secondary circuit for supplying an output to a load, and a synchronous rectifier having a control connection for opening and closing the synchronous rectifier, the improvement comprising:

a control circuit coupled between the control connections of the controllable switch and the synchronous rectifier comprising

(a) means for turning ON the synchronous rectifier in dependence on a voltage developed across a secondary winding on the main transformer, and

(b) means for turning OFF the synchronous rectifier in dependence on the first control signal turning ON the controllable switch.

APPENDIX B

Withdrawn Claims

1. A DC-DC flyback converter having a main transformer, a DC input connection in a primary circuit connected with a primary winding of the main transformer, a controllable primary switch in series with the primary winding of the main transformer, said controllable primary switch having a primary control signal input connection for applying a first control signal in controlling relation to the controllable primary switch, a load connection in a secondary circuit connected with a secondary winding of the main transformer, a synchronous rectifier connected in series with the secondary winding and having a control connection for applying a second control signal to the synchronous rectifier in controlling relation to the synchronous rectifier, a control circuit connected between the control signal input connection for applying the first control signal to the controllable switch and the control connection for applying the second control signal to the synchronous rectifier control connection; the improvement comprising:

the control circuit comprising a logic circuit having a voltage derived from the first control signal as a first input and a voltage derived from a secondary winding of the main transformer as a second input, the logic circuit being responsive to the voltage derived from a secondary winding of the main transformer to turn ON the synchronous rectifier and being responsive to the voltage derived from the first control signal to turn OFF the synchronous rectifier.

2. The flyback converter according to claim 1, wherein the logic circuit is connected to have a voltage derived from the voltage across the synchronous rectifier as a third input.

3. The flyback converter according to claim 2, wherein the logic circuit comprises an AND gate, the AND gate having an input to which the voltage derived from the first control signal is applied, a first bistable circuit having an output applied as a second input to the AND gate, a second bistable circuit having an output applied as a third input to the AND gate, the voltage derived from a secondary winding of the main transformer being applied as an input to a first comparitor having an output connected as an input to the first bistable circuit, the voltage derived from the voltage across the synchronous rectifier being applied as an input to a second comparitor having an output connected as an input to the second bistable circuit, and the first and second bistable circuits each having a further input to which is applied the voltage derived from the first control signal.

4. The flyback converter according to claim 3, wherein each of the first and second comparitors has a reference input set, in operation, at substantially 0 volts.

5. The flyback converter according to claim 3, wherein the first and second bistable circuits are first and second RS flip-flops, respectively, each having the voltage derived from the first control signal applied as an input to a "set" (S) input thereof, and the outputs of the first and second comparitors being applied respectively to "reset" (R) inputs of the first and second RS flip-flops, the first flip-flop having its "set" output (O) applied as an input to the AND gate and the second flip-flop having its "reset" output ($\overline{Q}$) applied as an input to the AND gate.

8. The method according to claim 6, further comprising:

(c) providing a logic circuit connected with a control electrode of the synchronous rectifier,

(d) applying a voltage derived from the voltage across a secondary winding as one input to the logic circuit, and

(e) applying a voltage derived from a main switch control signal as a further input to the logic circuit.

9. The method according to claim 8, further comprising:

(f) applying a voltage derived from a voltage across the synchronous rectifier as a third input to the logic circuit.

10. The method according to claim 9, wherein step (c) comprises:

(i) supplying the voltage derived from a main switch control signal as an input to an inverter,

(ii) providing an output of the inverter as an input to an AND gate,

(iii) supplying the voltage derived from a main switch control signal as an input to each of a first and a second bistable circuit,

(iv) applying a further input to the first bistable circuit upon the detection of a voltage across the secondary winding of the main transformer,

(v) applying another input to the second bistable circuit upon the detection of a voltage across the synchronous rectifier,

(vi) applying one output of the first bistable circuit as a further input to the AND gate,

(vii) applying one output of the second bistable circuit as another input to the AND gate, and

(viii) applying the output of the AND gate to the control electrode of the synchronous rectifier as a control signal turning ON and OFF the synchronous rectifier.

11. The method according to claim 10, further comprising providing first and second RS flip-flops as the first and second bistable circuits.

12. The method according to claim 11, wherein step (c) (iii) comprises applying the voltage derived from the main switch control signal to a "set" (S) input of each of the first and second RS flip-flops, step (c) (iv) comprises applying the further input to a "reset" (R) input of the first RS flip-flop, step (c) (v) comprises applying the another input to a "reset" (R) input of the second RS flip-flop, step (c) (vi) comprises applying a "set" (O) output of the first flip-flop to the AND gate, and step (c) (vii) comprises applying a "reset" (R) output of the second flip-flop to the AND gate.

17. The method according to claim 13, further comprising applying to the control primary winding a differential signal developed by differentiation of a main switch control signal.

18. The method according to claim 13, wherein the main switch control signal is substantially a square wave and applying a differential signal to the control primary comprises providing a differentiating RC circuit at an input to the control primary winding and applying the main switch control signal to the differentiating RC circuit.

19. The method according to claim 18, wherein applying the control voltage developed in the control secondary comprises applying the control voltage to a switching circuit connected in controlling relation to the synchronous rectifier.

20. The method according to claim 19, wherein the switching circuit is a transistor switching circuit connected to a control electrode of the synchronous rectifier and further

comprising deriving a DC bias, voltage from a secondary winding of the main transformer and applying the DC bias voltage to the transistor switching circuit.

21. The method according to claim 20, wherein the synchronous rectifier is a MOSFET switch and the transistor switching circuit is connected to a gate of the MOSFET switch.

22. The method according to claim 21, wherein the transistor switching circuit is a serially connected PNP and NPN transistor pair connected between the DC bias voltage and ground, a junction of the transistor pair being connected to the gate of the MOSFET switch.

25. The DC-DC flyback converter of claim 23, wherein the control circuit further comprises a differentiation circuit coupled between the primary control signal input connection and the control primary winding.

26. The DC-DC flyback converter of claim 25, wherein the primary control signal input connection applies a signal that is substantially a square wave in controlling relation to the controllable primary switch and to the differentiation circuit, whereby the differentiation circuit applies an input signal to the control primary winding that is substantially the differential of a square wave.

27. The DC-DC flyback converter of claim 26, further comprising a switching circuit operatively connected to the control secondary winding and connected in controlling relation to the synchronous rectifier.

28. The DC-DC flyback converter of claim 27, wherein the switching circuit is a transistor switching circuit connected in controlling relation to a control electrode of the synchronous rectifier.

29. The DC-DC flyback converter of claim 28, further comprising a DC bias circuit connected to provide DC bias to the transistor switching circuit, the DC bias circuit comprising a secondary winding on the main transformer and at least one rectifying diode.

30. The DC-DC flyback converter of claim 29, wherein the synchronous rectifier is a MOSFET switch and the transistor switching circuit is connected to a gate of the MOSFET switch.

31. The DC-DC flyback converter of claim 30, wherein the transistor switching circuit is a serially connected PNP and NPN transistor pair connected between the DC bias voltage and ground, a point of interconnection of the transistor pair being connected to the gate of the MOSFET switch.

32. The DC-DC flyback converter of claim 31, wherein one side of the control secondary winding output is connected to the base of each of the PNP and NPN transistors and another side of the control secondary winding output is connected to the point of interconnection of the transistor pair.

34. The DC-DC flyback converter of claim 33, wherein the control circuit is a logic circuit having as a first input the first control signal and having as a second input the voltage developed in the secondary winding.

35. The DC-DC flyback converter of claim 33, wherein the control circuit includes a control primary winding wound on the main transformer in addition to main primary and secondary windings and coupled to the controllable switch control connection by a differentiating circuit and a control secondary winding wound on the main transformer in addition to the control primary winding and the main primary and secondary windings and coupled to the synchronous rectifier control connection.

36. A DC-DC flyback converter having a main transformer, a primary circuit including a controllable switch connected in current controlling relation to a primary winding and having a control connection for opening and closing the switch under the control of a first control signal, a secondary circuit for supplying an output to a load, and a synchronous rectifier having a control connection for opening and closing the synchronous rectifier, the improvement comprising:

(a) a control primary transformer winding,

(b) a differentiation circuit coupling the control primary transformer winding to the first control signal, and

(c) a control secondary transformer winding coupled to the synchronous rectifier control connection to turn ON at a time subsequent to opening of the controllable switch and to turn OFF the synchronous rectifier substantially concurrently with the closing of the controllable switch.

37. The DC-DC flyback converter of claim 36, wherein the control primary winding and the control secondary transformer windings are wound on a core of the main transformer.

38. A DC-DC converter having a main transformer, a DC input connection in a primary circuit connected with a primary winding of the main transformer, a controllable primary switch in series with the primary winding of the main transformer, said controllable primary switch having a primary control signal input connection for applying a first control signal in controlling relation to the controllable primary switch, a load connection in a secondary circuit connected with a secondary winding of the main transformer, a synchronous rectifier connected in series with the secondary winding and having a control connection for secondary winding and having a control connection for inputting of a second control signal to the synchronous rectifier in controlling relation to the synchronous rectifier, a control circuit connected between the control signal input connection for applying the first control signal to the controllable switch and the control connection for inputting of the second control signal to the synchronous rectifier; the improvement comprising:

the control circuit having a rectified DC source including an auxiliary winding on the main transformer and a rectifier connected therewith for producing a DC voltage across a controlled transistor circuit, the controlled transistor circuit having a controlling input from a control circuit secondary transformer winding, a control circuit primary transformer winding inductively coupled to the control circuit secondary winding, and a derivative circuit connected between the primary control signal input connection and the control circuit primary winding, the derivative circuit being adapted to supply to the control circuit primary winding a derivative with time of the first control signal.

APPENDIX C

Evidence, 37 C.F.R. § 41.37(c) (1) (ix), None.

APPENDIX D

Related Proceedings, 37 C.F.R. § 41.37 (c) (1) (x)

There are no decisions rendered by a court or the Board in any proceeding.

SEQUENTIAL MACHINE

For articles on related subjects see AUTOMATA THEORY; BOOLEAN ALGEBRA; FORMAL LANGUAGES; PROBABILISTIC AUTOMATA; REGULAR EXPRESSION; and SWITCHING THEORY.

Basic Concepts

A *sequential machine* is a mathematical model of a certain type of simple computational structure. If a sequential machine has a finite number of states, it is frequently called a *finite-state machine*, or FSM. Sequential machines have numerous applications, for example, in asynchronous circuits, coding theory, concurrent systems, digital circuit design, formal language theory, hardware testing, protocol design, and software and hardware verification.

There are several varieties of sequential machine, of which the most common is the finite-state, synchronous sequential machine. It has an input σ, which can take on any value from a finite set Σ, called the *input alphabet*, and an output δ, from a finite *output alphabet* Δ, as shown in Fig. 1. The input and output values are of interest only at certain instants of time, which are usually identified with the integers $1, 2, 3, \ldots$. At any time t, the output $\delta(t)$ depends not only on the present input $\sigma(t)$ (as is the case in combinational circuits), but also on the past input *sequence* $\ldots, \sigma(t-k), \sigma(t-k+1), \ldots, \sigma(t-1)$; hence the name *sequential machine*. In this section we shall, for simplicity, assume that $k = 0$.

The dependence of the output on past inputs implies that a sequential machine has memory. Usually, this memory is finite and corresponds to a finite set Q, called the set of *internal states*. At time t machine M is in some (present) internal state $q(t)$. It receives an input value $\sigma(t)$, and this present input and present internal state determine the next internal state $q(t+1)$.

An example of a sequential machine is shown in Fig. 2. The machine is represented by a directed graph, its *state graph*, where the nodes correspond to internal states and the labeled edges to transitions among internal states. The labels are of the form σ/δ, where σ is the input value causing the transition and δ is the corresponding output value. For example, if M_1 of Fig. 2 is in state q_1 at time t, and if $\sigma(t) = 1$, then the transition labeled 1/0 is relevant;the output produced during the transition is $\delta(t) = 0$, and the next state of M_1 is $q(t+1) = q_2$. In general, if we are given an initial state $q(1)$ (i.e. the value of q at $t = 1$), and

Figure 1. Sequential machine block diagram.

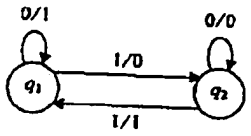


Figure 2. Machine M_1.

an input sequence $\sigma(1), \ldots, \sigma(t)$, we can determine from the state graph the resulting state sequence $q(2), \ldots, q(t+1)$ and the corresponding output sequence $\delta(1), \ldots, \delta(t)$. A typical computation is shown in Table 1, where it is assumed that $q(1) = q_1$. The reader will verify that, if M_1 is started in state q_1, it will produce an output of 1 at time t if and only if the number of 1s in the sequence $\sigma(1), \ldots, \sigma(t)$ is even.

With each sequential machine we associate two functions: the *transition function* f, which determines the next state from the present state and the present input, and an *output function* g. In machine M_1, the present output depends on both the present state and the present input. Such a model, in which $\delta(t) = g(q(t), \sigma(t))$, is called the *Mealy model*. In another useful model, the *Moore model*, the present output is uniquely determined by the present state, i.e. $\delta(t) = g(q(t))$.

An example of a Moore machine is shown in Fig. 3. The input and output alphabets are $\Sigma = \{a, b\}$ and $\Delta = \{0, 1, 2\}$, respectively. Given an initial state and an input sequence, we can determine the state sequence, as in the Mealy model. Since the output is determined solely by the state, we associate it with the nodes of the state graph rather than with the edges. A typical computation for M_2 is shown in Table 2, assuming $q(1) = q_1$. The behavior of M_2 can be described as follows: the input value a is "ignored" by M_2, in the sense that no change of state results when $\sigma(t) = a$. The input b advances the state of M_2 cyclically. If the machine is started in q_1, the output $\delta(t+1)$ is congruent modulo 3 to the number of bs in the input sequence $\sigma(1), \ldots, \sigma(t)$.

Table 1. Sequences for M_1.

Time:	1	2	3	4	5	6	7
Input:	0	1	0	0	1	1	
State:	q_1	q_1	q_2	q_2	q_2	q_1	q_2
Output:	1	0	0	0	1	0	

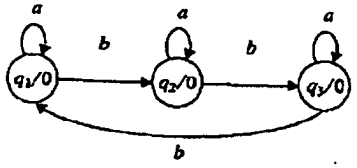


Figure 3. Machine M_2.

Table 2. Sequences for M_2.

Time:	1	2	3	4	5	6	7
Input:	b	a	b	a	b	b	
State:	q_1	q_2	q_2	q_3	q_3	q_1	q_2
Output:	0	1	1	2	2	0	1

The differences between Moore and Mealy models are only technical. From a general point of view, these models are equivalent as far as computational power is concerned. Another related model is the *finite automaton*. This is a special case of the Moore machine, where $\Delta = \{0, 1\}$. If the output corresponding to an internal state is 1, that state is called *accepting*, or *final*; if the output is 0, the state is called *rejecting*. A single initial state q_0 is usually specified in a finite automaton A, which can then can be viewed as an *acceptor* of input sequences. For the input sequence $\sigma(1), \ldots, \sigma(t)$, let $q(t+1)$ be the state reached by A, when it is started in q_0. If $q(t+1)$ is a final state, the sequence is accepted; otherwise, it is rejected.

An alternative point of view considers a sequential machine as a *sequence transducer*—a machine that transforms an input sequence into an output sequence, as in Tables 1 and 2.

Realization of Sequential Machines

The behavior of a sequential machine can be realized by a sequential switching circuit. We now describe an idealized model of such a circuit. The *sequential network* model reflects the logical properties of the switching circuit, but not its electronic properties. Thus it has the advantage of being independent of the actual technological implementation, while retaining many of the basic structural properties.

A block diagram of a sequential network is shown in Fig. 4. As is usually the case, we assume that all signals in a sequential network are binary, with 0 and 1 as the two possible values. The network has a finite number of binary inputs $x_1, \ldots, x_n$ and binary outputs $z_1, \ldots, z_m$. If the output values $z_j(t)$ at time t are uniquely determined by the input values $x_j(t)$, then it has no memory. In that case, it is called a *combinational network*, and its behavior can be described by m Boolean functions, one for each output z_j. A combinational network can be implemented by a network of logic gates *without* any feedback loops.

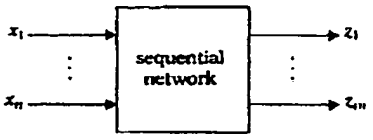


Figure 4. Sequential network.

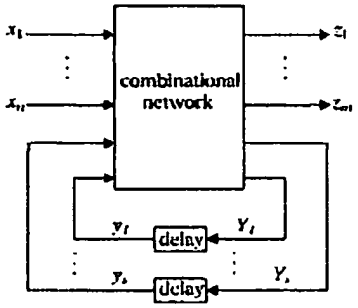


Figure 5. Sequential network with unit delays.

A switching network with memory is called *sequential*. The function of memory can be performed by gate networks *with* feedback. In general, such networks have no special timing signals and are called *asynchronous*. If a special periodic input, called *clock*, is provided to control the action of the network, the network is *synchronous*. In that case, the response of the network is of interest only at certain times, once during each clock period. These times correspond to the instants $1, 2, \ldots$ mentioned earlier.

A synchronous sequential network can be divided into a combinational part and a memory part. The units corresponding to memory are asynchronous networks called *flip-flops*. For theoretical considerations, the simplest memory module is the *unit delay*, whose output y is equal to the input x delayed by one unit of time; i.e., $y(t) = x(t-1)$. The general form of a synchronous sequential network with unit delays as memory elements is shown in Fig. 5. The network can be described by two sets of equations.

1. Next-state equations: for $i = 1, \ldots, s$,

$$y_i(t+1) = Y_i(t) = f_i(x_1(t), \ldots, x_n(t), y_1(t), \ldots, y_s(t)).$$

2 Output equations: for $j = 1, \ldots, m$,

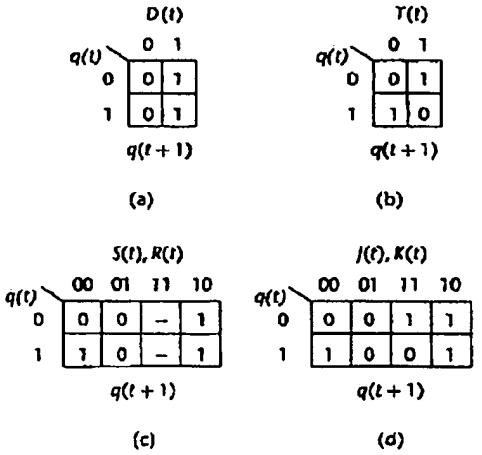
$$z_j(t) = g_j(x_1(t), \ldots, x_n(t), y_1(t), \ldots, y_s(t)).$$

The f_i in (1) and the g_j in (2) are Boolean functions.

The reader will easily verify that the sequential network model of Fig. 5 is a special case of the Mealy model, where Σ is the set of all binary n-tuples (binary words of length n), Δ is the set of all binary m-tuples, and Q is the set of all binary s-tuples.

Any abstract sequential machine can be realized by a sequential network of the type shown in Fig. 5. This can be done by representing each element of Σ by a suitable n-tuple $x_1, \ldots, x_n$, and Δ and Q must be coded similarly.

Table 3. State tables for flip-flops: (a) D flip-flop, (b) T flip-flop, (c) SR flip-flop, (d) JK flip-flop. Each table shows the value of $q(t+1)$.



The unit delay is sometimes called the *D flip-flop*. Other types of flip-flops are the T (*toggle* or *trigger*) type, the SR (*set–reset*) type, and the JK type. In Table we define the four types of flip-flops by their *state tables*, which constitute a common way (equivalent to the state-graph) of representing sequential networks. The rows of the state table correspond to the internal states, and the columns to input combinations. The entries represent the next state. The most general type of flip-flop is the JK. The condition $J = 0, K = 0$ is the *remember* condition, where no change takes place; $J = 0, K = 1$ corresponds to the *reset* condition (the flip-flop is reset to 0); $J = 1, K = 0$ is the *set* condition; and $J = 1, K = 1$ is the *toggle* condition (the state changes, or *toggles*). The combination 11 is not used in an SR flip-flop. Any sequential machine can be realized using logic gates and flip-flops of any one of the four types.

Behavioral Properties

Two states q and q' of a sequential machine M are *indistinguishable* if the input–output (I/O) behavior of M started in q cannot be distinguished by any external experiment from that of M started in q'. In other words, any input sequence applied to M started in q, produces the same output sequence as in the case when M is started in q'. Otherwise, q and q' are *distinguishable*. A sequential machine in which any two states are distinguishable is called *reduced*.

Two sequential machines M and M' are indistinguishable if for every state q of M there exists a state q' of M' such that the I/O behavior of M started in q is the same as that of M' started in q', and vice versa. For every sequential machine M, there exists a unique (up to isomorphism) reduced sequential machine M_0 indistinguishable from M. Machine M_0 is the *minimal-state version* of M.

A set of sequences over a finite alphabet is called a *language*. It is useful to associate certain languages with sequential machines. For example, in the case of a finite automaton A, we define the *language* $L(A)$ of A to be the set of all accepted sequences. Similarly, the set L_{ij} of all sequences taking a sequential machine from state q_i to state q_j, or the set L_δ, of all sequences resulting in a particular output value δ, represent useful languages. All such languages of the form $L(A)$, L_{ij}, or L_δ are *regular languages*. It can be shown that any language defined by a sequential machine in the sense given above is regular, and, conversely, for every regular language there exists a sequential machine "recognizing" that language.

One basic function of sequential machines is counting. When the number of states is finite, a sequential machine can only count "up to a threshold" (see below) and then modulo an integer.

Another unique characterization of sequential machines is provided by the *syntactic semigroup* of the machine, defined as follows: for each input σ, the set Q of states of a reduced machine is transformed according to the transition function. The set of all transformations of states performed by all input sequences constitutes the syntactic semigroup. This representation is useful for certain structural properties.

Structural Properties

In a general network, as shown in Fig. 5, there may be *feedback loops*. For example, Y_1 may be a function of y_2, and Y_2 may be a function of y_1. In the special case where no such loops exist, the network is called *definite*. An example of a simple definite network is shown in Fig. 6, where the rectangles represent unit delays. The languages recognized by definite networks are particularly simple, since the behavior of such networks depends only on the last k symbols of the input sequence, for some k. In general, feedback is required to realize the behavior of an arbitrary sequential machine. It can be shown, however, that every sequential machine can be realized by a sequential network having a single feedback loop.

When SR flip-flops (instead of unit delays) are used as memory elements, the class of machines realizable without feedback is considerably larger than the class of definite machines. The languages recognized by

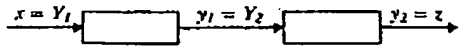


Figure 6. A definite machine.

machines in this class are the so-called *noncounting* regular languages. Such machines can only count to a threshold in the following sense: if the threshold is the integer $k \geq 0$, then the machine may be able to determine whether a certain sequence of symbols occurs in the input sequence $0, 1, \ldots,$ or $k-1$ times. After this, it cannot distinguish k occurrences from $k+1$ occurrences, but can only conclude that the number of occurrences is at least k. Therefore, such machines cannot count modulo any integer greater than one, and are called *counter-free*. The languages corresponding to counter-free machines constitute a natural subclass of regular languages. They can be defined by regular expressions that use only Boolean operations and concatenation. Such expressions are called *star-free*. The syntactic semigroups corresponding to this class of machines and languages are *group-free* (i.e. contain only subgroups of order 1).

Sequential machines that can be realized by networks of unit delays and exclusive-OR gates are *linear* and constitute a proper subclass of sequential machines. Linear machines have important applications in coding theory, and also in circuit testing.

The problem of decomposing a sequential machine into a *cascade connection* of smaller sequential machines has received much attention. The cascade connection of two machines is shown in Fig. 7. This connection is also known as the *series connection*. The *parallel connection* of two machines is a special case of the cascade connection, where neither machine influences the other. We have already indicated that definite machines correspond to cascade connections of unit delays (*see* Fig. 6), and counter-free machines correspond to cascade connections of *SR* flip-flops. The Krohn–Rhodes theory shows that, in general, arbitrary sequential machines correspond to cascade connections of machines whose syntactic semigroups are simple groups, and *SR* flip-flops. Such results are of theoretical interest. For practical applications, an often-used connection is a *shift register*, which is a very simple cascade connection of flip-flops, used, for example in a computer connection to a serial communication line. Shift registers and counters constitute basic modules in the design of sequential networks.

Related Models

In practical applications, certain state-input combinations of a sequential machine may never occur. In this case, the next state and output may be irrelevant and need not be specified. The *incompletely specified* sequential machine model handles such cases.

The situation where the next state and output of a machine are not precisely predictable is modeled by *stochastic* or *probabilistic* sequential machines. The case where the transition and output functions vary with time is modeled by *time-varying* sequential machines. Stochastic and time-varying machines are both more powerful than ordinary machines in the sense that they can recognize some languages that are not regular.

A theoretically convenient model is the *nondeterministic* sequential machine. Here, for a given present state and input, the next state can be chosen from a set of states; i.e. it is not necessarily unique. As acceptors of languages, nondeterministic machines are no more powerful than deterministic machines; both types can recognize only regular languages. A nondeterministic machine can have fewer states than the corresponding reduced deterministic machine accepting the same language.

The concept of a *generalized sequential machine* (GSM) has applications in the theory of formal languages. In this model, for a given present state and input symbol, the machine can produce a sequence of output symbols, whereas the standard model permits only one output symbol. The GSM is also a more powerful model than the standard one.

In the discussion above, we have assumed that the term *sequential machine* implies that the number of states is finite. *Infinite-state* sequential machines have also been studied. They are obviously much more powerful than finite-state machines, and most of the results discussed above do not apply directly to the infinite-state case. Infinite-state linear sequential machines provide an example, in which a number of results from the finite-state case have their generalized counterparts in the infinite case. Finite-state machines can also operate on infinite strings. Such machines have applications to mathematical logic and to processes, such as operating systems, where nonterminating computations are used.

Sequential machines are widely used to verify hardware designs and computer programs which use only a finite amount of memory. Symbolic *model checking* (*q.v.*) is a method in which sets of states, rather than individual states, are analyzed. This leads to efficient algorithms that overcome the "state explosion" problem (the number of states is exponential in the number of system variables).

Sequential machines are also very useful in the design and verification of computer protocols (*q.v.*). In

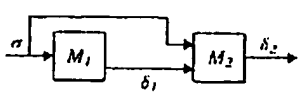


Figure 7. Cascade connection.

particular, concurrent processes can be represented as *communicating* finite-state machines. *Extended* finite-state machines are more versatile, since they permit variables, which can be used to control state transitions. Special models such as *Petri nets* (*q.v.*) and *FIFO nets* are also used in this area.

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